

***In the Claims:***

These claims replace all prior versions and listings of claims in the above-referenced application.

1           1. - 15. (Canceled)

1           16.     (Currently Amended) An apparatus comprising:  
2           a multiply accumulate (MAC) unit coupled to operand busses at respective  
3 operand inputs, the MAC unit configured to latch a first multiple-bit data value during  
4 a first cycle and execute the MAC functions on the first multiple-bit data value during  
5 the next subsequent cycle while latching a second multiple-bit data value, the MAC  
6 unit further configured to supply a first MAC result responsive to the first multiple-bit  
7 data value on a result bus once the first MAC result is available and latch a second  
8 MAC result responsive to the second multiple-bit data value;  
9           a register coupled to the result bus and configured to latch the first MAC  
10 result; and  
11          a miscellaneous logic unit coupled between the result bus and the register, the  
12 miscellaneous logic unit configured to perform logical operations not requiring  
13 multiply accumulate functions, the miscellaneous logic unit further configured to  
14 generate first and second control signals responsive to at least one certain exceptional  
15 condition, wherein when the first control signal is asserted the MAC unit supplies the  
16 second MAC result on the result bus, when the second control signal is asserted the  
17 first MAC result is driven from the register onto the result bus, and wherein when the  
18 second control signal is not asserted a miscellaneous-unit generated result is driven  
19 onto the result bus.

1           17.     (Currently Amended) The apparatus of claim 16, wherein the  
2 miscellaneous logic unit is configured to identify ~~and~~ an exceptional condition  
3 responsive to an operand.

1           18.   (Previously Presented) The apparatus of claim 16, wherein the  
2   miscellaneous logic unit is configured to recognize an exceptional condition identified  
3   by the MAC unit.

1           19.   (Previously Presented) The apparatus of claim 18, wherein the  
2   miscellaneous logic unit directs the replacement of one of the first and second MAC  
3   results with a representation of the exceptional condition.

1           20.   (Currently Amended) A method for performing single-instruction  
2   multiple-data instructions comprising:  
3           applying a plurality of data values on an operand bus for two consecutive  
4   cycles;  
5           latching a first data value in a multiply accumulate (MAC) unit during a first  
6   cycle;  
7           initiating execution of the multiply and accumulate functions on the first data  
8   value and latching a second data value in the MAC unit during a second cycle;  
9           deferring a first MAC unit result responsive to the first data value;  
10          initiating execution of the multiply and accumulate functions on the second  
11   data value during a cycle subsequent to the second cycle to generate a second MAC  
12   unit result; and  
13          using a miscellaneous logic unit configured to perform logical operations not  
14   requiring multiply accumulate functions to generate ~~generating~~ a plurality of control  
15   signals responsive to the first data value, the second data value, and an exceptional  
16   condition when identified by the MAC unit.

1           21.   (Previously Presented) The method of claim 20, further comprising  
2   applying the plurality of control signals to arrange a combination selected from the  
3   first MAC unit result, the second MAC unit result, and a representation of an  
4   exceptional condition.

1           22.   (Previously Presented) The method of claim 20, wherein deferring  
2   comprises forwarding the first MAC unit result to a register.

1           23.   (Previously Presented) The method of claim 20, wherein generating  
2   comprises determining when an operand is invalid.

1           24.   (Previously Presented) The method of claim 20, wherein generating  
2   comprises determining when an operation in combination with an operand will  
3   produce an exceptional condition.

1           25.   (Previously Presented) The method of claim 20, further comprising  
2   forwarding the combination to a result bus.

1           26.   (Currently Amended) An apparatus comprising:  
2       means for producing a plurality of control signals responsive to a first data  
3   value, a second data value, and an exceptional condition, wherein the exceptional  
4   condition results from the execution of a multiply accumulate (MAC) unit over the  
5   first and second data values, the means for producing configured to perform logical  
6   operations not requiring multiply accumulate functions; and  
7       means for arranging a combination selected from a first MAC unit result, a  
8   second MAC unit result, and a representation of the exceptional condition responsive  
9   to the plurality of control signals.

1           27.   (Previously Presented) The apparatus of claim 26, wherein the first  
2   MAC unit result is responsive to the first data value.

1           28.   (Previously Presented) The apparatus of claim 26, wherein the second  
2   MAC unit result is responsive to the second data value.

1           29.   (Previously Presented) The apparatus of claim 26, wherein the  
2   exceptional condition is identified by the MAC unit.

1           30.   (Previously Presented) The apparatus of claim 26, wherein the  
2   exceptional condition is identified by the means for producing the plurality of control  
3   signals responsive to at least one of the first and second data values and an opcode.